WHAT IS CLAIMED IS:

1. A switched capacitor amplifier circuit, comprising:

an operational amplifier;

a plurality of switch circuits;

a plurality of capacitors; and

two input terminals;

wherein a standard voltage and a reference voltage are provided, and noise components of the standard voltage and the reference voltage are made in phase to reduce noises caused by offset voltage adjustment.

2. A switched capacitor amplifier circuit, comprising:

a first input terminal to which a first input signal is inputted;

a second input terminal to which a second input signal is inputted;

a first capacitor to which a signal based on an output of the first input terminal is inputted;

a second capacitor to which a signal based on an output of the second input terminal is inputted;

an operational amplifier that compares a signal based on an output of the first capacitor with a signal based on an output of the second capacitor to output a signal;

a first reference voltage terminal to which a first reference

voltage that supplies electric charges to the first capacitor is applied; and

a second reference voltage terminal to which a second reference voltage that supplies electric charges to the second capacitor is applied,

wherein at least one of the first reference voltage and the second reference voltage is adjusted so that a difference between the first reference voltage and the second reference voltage coincides with an offset voltage between the first input terminal and the second input terminal.

3. A switched capacitor amplifier circuit as claimed in claim 2, wherein the first reference voltage has a temperature characteristic, and

when an offset voltage between the first input terminal and the second input terminal has the temperature characteristic, the first reference voltage sets the temperature characteristic so that a difference in voltage value between the first reference voltage and the second reference voltage coincides with the offset voltage between the first input terminal and the second input terminal.

4. A switched capacitor amplifier circuit, comprising:

an operational amplifier;

first and second capacitors and a first switch circuit each

having one end connected to one of input terminals of the operational amplifier, respectively;

third and fourth capacitors and a second switch circuit each having one end connected to one of input terminals of the operational amplifier, respectively;

third and fourth switch circuits each having one end connected to the other end of the first capacitor;

fifth and sixth switch circuits each having one end connected to the other end of the third capacitor;

a first reference voltage connected to the other end of the third switch circuit;

a second reference voltage connected to the other end of the fifth switch circuit;

seventh and eighth switch circuits each having one end connected to the other end of the second capacitor;

ninth and tenth switch circuits each having one end connected to the other end of the fourth capacitor;

an eleventh switch circuit and a fifth capacitor which are connected to the other end of the first switch circuit; and

a twelfth switch circuit and a sixth capacitor which are connected to the other end of the second switch circuit;

wherein the other end of the fifth capacitor and the other end of the second switch circuit are connected to the output terminal of the operational amplifier,

the other end of the eight switch circuit, the other end of the tenth switch circuit, the other end of the eleventh switch circuit and the other end of the twelfth switch circuit are connected to the second reference voltage, and

the other ends of the fourth and sixth switch circuits are input terminals.

5. An electronic device having the switched capacitor amplifier circuit as claimed in claim 4.

6. An electronic device having the switched capacitor amplifier circuit as claimed in claim 3.

7. An electronic device having the switched capacitor amplifier circuit as claimed in claim 2.

8. An electronic device having the switched capacitor amplifier circuit as claimed in claim 1.